

forming a connecting hole at a predetermined position of the insulating film through the insulating film so as to expose the first conducting layer therein;

forming a barrier metal layer of at least one of tungsten nitride WN and tungsten silicide nitride WSiN, said WN forming when performed being performed with a first thermal CVD process under the following conditions,

WF₆ gas: 5-80 sccm,

N-containing gas: present,

Temperature: 300-450°C, and

Pressure: 0.5-80 Torr, and

said WSiN forming when performed being performed with a second thermal CVD method under the following conditions,

WF₆ gas: 2-20 sccm,

Si-containing gas including SiH₄: 10-300 sccm,

N-containing gas: present,

Temperature: 300-650°C, and

Pressure: 0.7-80 Torr,

wherein the forming a barrier metal layer deposits said barrier metal layer on an inner surface of the connecting hole, a surface of the first conducting layer exposed in a bottom portion of the connecting hole, and an upper surface of the insulating film; and

depositing a metal film on the barrier metal layer and simultaneously filling the connecting hole with the metal film, thereby forming a second conducting layer electrically connected with the first conducting layer via the barrier metal.

64. (New) The method according to claim 63, wherein the insulating film is an interlayer insulating film.

65. (New) The method according to claim 64, wherein at least one of the first and second conducting layers is formed of Cu and the interlayer insulating film is formed any one of SiO₂, SiOF, Ta₂O₅, and CF_x (x=1-4).

66. (New) The method according to claim 63, wherein the connecting hole is a via-hole.

67. (New) The method according to claim 63, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, Cu, and Si; and another one of the first conducting layer and the second conducting layer is formed of any one of W, Cu, and Al, Si.

68. (New) A method of forming a wiring structure of a semiconductor device, comprising:

forming an insulating film on a semiconductor substrate having a first conducting layer;

forming a connecting hole at a predetermined position of the insulating film through the insulating film so as to expose the first conducting layer therein;

forming a barrier metal layer of at least one of tungsten nitride WN and tungsten silicide nitride WSiN, said WN forming when performed being performed with a first thermal CVD process under the following conditions,

WF₆ gas: 5-80 sccm,

N-containing gas: present,

Temperature: 300-450°C, and

Pressure: 0.5-80 Torr, and

said WSiN forming when performed being performed with a second thermal CVD method under the following conditions,

WF₆ gas: 2-20 sccm,

Si-containing gas including SiH₄: 10-300 sccm,

N-containing gas: present,

Temperature: 300-650°C, and

Pressure: 0.7-80 Torr,

wherein the forming a barrier metal layer of at least one of tungsten nitride WN and tungsten silicide nitride WSiN uses CVD from an inner surface of the connecting hole to a surface of the first conducting layer exposed in a bottom portion of the connecting hole and to an upper surface of the insulating film; and

depositing a metal film on the barrier metal layer and simultaneously filling the connecting hole with the metal film, thereby forming a second conducting layer electrically connected with the first conducting layer via the barrier metal.

69. (New) The method according to claim 68, wherein the connecting hole is a contact hole.

70. (New) The method according to claim 68, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, and Cu and the other one of the first conducting layer and the second conducting layer is formed of Si, Cu, Al, and W.

71. (New) The method according to claim 68, wherein at least one of the first and second conducting layers is formed of Cu and the insulating film is formed any one of SiO₂, SiOF, Ta₂O₅, and CF_x (x=1-4).

72. (New) A method of forming a wiring structure of a semiconductor device, comprising:

forming an insulating film on a semiconductor substrate;

forming a wiring portion and a connecting hole simultaneously at a predetermined position of the insulating film through the insulating film so as to expose the first conducting layer;

forming a barrier metal layer of at least one of tungsten nitride WN and tungsten silicide nitride WSiN, said WN forming when performed being performed with a first thermal CVD process under the following conditions,

WF₆ gas: 5-80 sccm,

N-containing gas: present,

Temperature: 300-450°C, and

Pressure: 0.5-80 Torr, and

said WSiN forming when performed being performed with a second thermal CVD method under the following conditions,

WF₆ gas: 2-20 sccm,

Si-containing gas including SiH₄: 10-300 sccm,

N-containing gas: present,

Temperature: 300-650°C, and

Pressure: 0.7-80 Torr,

wherein the forming a barrier metal layer uses CVD from inner surfaces of the wiring portion and the connecting hole to a surface of the first conducting layer exposed in a bottom portion of the connecting hole and to an upper surface of the insulating film;

depositing a metal film on the barrier metal layer and simultaneously filling the connecting hole with the metal film, thereby forming a second conducting layer electrically connected with the first conducting layer via the barrier metal; and

removing a residual metal film of the second conducting layer, thereby flattening the

second conducting layer.

73. (New) The method according to claim 72, wherein a dual damascene structure is formed of the wiring portion and the connecting hole.

74. (New) The method according to claim 72, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, and Cu, and the other one of the first conducting layer and the second conducting layer is formed of any one of Si, Cu, W and Al.

75. (New) The method according to claim 72, wherein the insulating film is formed of any one of SiO_2 , SiOF_x , Ta_2O_5 , and CF_x ($x=1-4$).

76. (New) The method according to claim 72, wherein the metal film of the second conducting layer is flattened by CMP.

77. (New) The method according to claims 63, 68, or 72, wherein the N-containing gas is any one of NH_3 , MMH, N_2 , and a mixture of these elements.

78. (New) The method according to claim 77, wherein, when NH_3 is used as the N-containing gas and the WSi is purged with an inert gas before the nitriding is performed.

79. (New) A method of forming a gate electrode of a transistor formed on a semiconductor substrate, comprising:

forming a barrier metal layer of at least one of tungsten nitride WN and tungsten silicide nitride WSiN on a gate oxide film located between a drain and source of a transistor, said WN forming when performed being performed with a first thermal CVD process under the following conditions,

WF_6 gas: 5-80 sccm,

N-containing gas: present,

Temperature: 300-450°C, and

Pressure: 0.5-80 Torr, and

said WSiN forming when performed being performed with a second thermal CVD method under the following conditions,

WF₆ gas: 2-20 sccm,

Si-containing gas including SiH₄: 10-300 sccm,

N-containing gas: present,

Temperature: 300-650°C, and

Pressure: 0.7-80 Torr; and

forming a metal layer on the barrier metal layer.

80. (New) A method of forming a gate electrode of a transistor formed on a semiconductor substrate; comprising:

forming a polysilicon layer on a gate oxide film formed between a source and a drain of a transistor;

forming a barrier metal layer of at least one of tungsten nitride WN and tungsten silicide nitride WSiN, said WN forming when performed being performed with a first thermal CVD process under the following conditions,

WF₆ gas: 5-80 sccm,

N-containing gas: present,

Temperature: 300-450°C, and

Pressure: 0.5-80 Torr, and

said WSiN forming when performed being performed with a second thermal CVD method under the following conditions,

WF₆ gas: 2-20 sccm,

Si-containing gas including SiH₄: 10-300 sccm,

N-containing gas: present,

Temperature: 300-650°C, and

Pressure: 0.7-80 Torr; and

forming a metal film on the barrier metal layer.

81. (New) The method according to claims 79 or 80, wherein the metal layer comprises at least one of W, Cu, and Al.

82. (New) The method according to claims 79 or 80, wherein the gate oxide film comprises any one of SiO₂, SiOF, Ta₂O₅, and CF_x (x=1-4).

83. (New) The method according to claims 79 or 80, wherein the N-containing gas is any one of NH₃, MMH, N₂, and a mixture of these elements

84. (New) The method according to claim 83, wherein, when NH₃ is used as the containing gas, the WSi is purged with an inert gas before the nitriding is performed.

85. (New) The method according to any one of claims 63, 68, 72, and 79-80, wherein said WN has a W:N ratio of 1:0.5-1.0 and said WSiN has a W:Si:N ratio of 1 : 0.02-0.2 : 0.02-0.2, and the gas containing Si is any one of SiH₄, Si₂H₆, and SiH₂Cl₂.

86. (New) The method according to any one of claims 63, 68, 72, and 79-80, wherein the Si-containing gas is any one of SiH₄, Si₂H₆, and SiH₂Cl₂.

87. (New) The method according to any one of claims 63, 68, 72, and 79-80, further comprising:

removing gasses for forming a W film by supplying an inert gas into a reaction vessel between the step of forming a W film and the step of nitriding the W film.

88. A method of forming a barrier metal layer of at least one of tungsten nitride WN and tungsten silicide nitride WSiN, comprising at least one of:

forming said WN with a first thermal CVD process under the following conditions,

WF₆ gas: 5-80 sccm,
N-containing gas: present,
Temperature: 300-450°C, and
Pressure: 0.5-80 Torr; and
forming said WSiN with a second thermal CVD method under the following
conditions,

WF₆ gas: 2-20 sccm,
Si-containing gas including SiH₄: 10-300 sccm,
N-containing gas: present,
Temperature: 300-650°C, and
Pressure: 0.7-80 Torr.

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 63-88 are presently active; Claims 28-62 having been canceled, and Claims 63-88 having been added by way of the present amendment.

In the Office Action, Claims 36-42 and 57-62 were rejected under 35 U.S.C. §103(a) (IEDM 94-497, pp. 19.4.1-19.4.2) as being unpatentable over Agnello et al (U.S. Patent No. 5,796,166) or Kasai et al taken with Fleming et al (U.S. Pat. No. 5,916,634). Claims 38, 41, and 59 were rejected under 35 U.S.C. §103(a) as being unpatentable over Agnello et al or Kasai et al taken with Fleming et al and further in view of Wolf et al ("Silicon Processing for the VLSI ERA"; vol. 2, Lattice Press). Claims 39, 42, and 60 were rejected under 35 U.S.C. §103(a) as being unpatentable over Agnello et al or Kasai et al taken with Fleming et al and